

Dual LDO with Low Noise, Very High PSRR and Low I_Q

ISL9000A is a high performance dual LDO capable of sourcing 300mA current from each output. It has a low standby current and very high PSRR and is stable with output capacitance of 1 μ F to 10 μ F with ESR of up to 200m Ω .

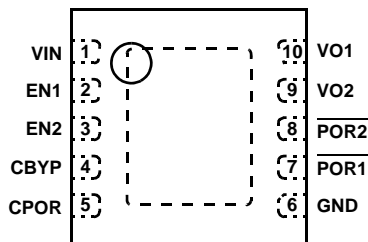
The device integrates an individual Power-On-Reset (POR) function for each output. The POR delay for VO2 can be externally programmed by connecting a timing capacitor to the CPOR pin. The POR delay for VO1 is internally fixed at approximately 2ms. A reference bypass pin is also provided for connecting a noise filtering capacitor for low noise and high-PSRR applications.

The quiescent current is typically only 42 μ A with both LDO's enabled and active. Separate enable pins control each individual LDO output. When both enable pins are low, the device is in shutdown, typically drawing less than 0.1 μ A.

Several combinations of voltage outputs are standard. Output voltage options for each LDO range from 1.5V to 3.3V. Other output voltage options may be available upon request.

Pinout

ISL9000A
(10 LD 3X3 DFN)
TOP VIEW



Features

- Integrates two 300mA high performance LDOs
- Excellent transient response to large current steps
- $\pm 1.8\%$ accuracy over all operating conditions
- Excellent load regulation: < 0.1% voltage change across full range of load current
- Low output noise: typically 30 μ V_{RMS} @ 100 μ A (1.5V)
- Very high PSRR: 90dB @ 1kHz
- Extremely low quiescent current: 42 μ A (both LDOs active)
- Wide input voltage capability: 2.3V to 6.5V
- Low dropout voltage: typically 200mV @ 300mA
- Stable with 1 μ F to 10 μ F ceramic capacitors
- Separate enable and POR pins for each LDO
- Soft-start and staged turn-on to limit input current surge during enable
- Current limit and overheat protection
- Tiny 10 Ld 3mmx3mm DFN package
- -40°C to +85°C operating temperature range
- Pb-free (RoHS compliant)

Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Handheld Devices including Medical Handheld

Ordering Information

PART NUMBER (Notes 1, 3)	PART MARKING	VO1 VOLTAGE (V) (Note 2)	VO2 VOLTAGE (V) (Note 2)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL9000AIRNNZ	DEYA	3.3	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRNJZ	DEWA	3.3	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRNFZ	DEVA	3.3	2.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRNCZ	DETA	3.3	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRMNZ	DESA	3.0	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRMMZ	DERA	3.0	3.0	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRMGZ	DEPA	3.0	2.7	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRLLZ	DENA	2.9	2.9	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKNZ	DELA	2.85	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKKZ	DEKA	2.85	2.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKJZ	DEJA	2.85	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKFZ	DEHA	2.85	2.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKPZ	DEMA	2.85	1.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKCZ	DEGA	2.85	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJNZ	DEEA	2.8	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJMZ	DEDA	2.8	3.0	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJRZ	DEFA	2.8	2.6	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJCZ	DECA	2.8	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJBZ	DEBA	2.8	1.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRGPZ	DDYA	2.7	1.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRGCZ	DDWA	2.7	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRFJZ	DDVA	2.5	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRFDZ	DDTA	2.5	2.0	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRFCZ	DDSA	2.5	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRPLZ	DFBA	1.85	2.9	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRPPZ	DFCA	1.85	1.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRCJZ	DDRA	1.8	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRCCZ	DDPA	1.8	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRBLZ	DDNA	1.5	2.9	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRBJZ	DDMA	1.5	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRBCZ	DDLA	1.5	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRBBZ	DDKA	1.5	1.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C

NOTES:

1. Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. For other output voltages, contact Intersil Marketing.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

ISL9000A

Absolute Maximum Ratings

Supply Voltage (VIN)	+7.1V
VO1, VO2 Pins	+3.6V
All Other Pins	-0.3 to (VIN + 0.3)V

Recommended Operating Conditions

Ambient Temperature Range (TA)	-40°C to +85°C
Supply Voltage (VIN)	2.3V to 6.5V

Thermal Information

Thermal Resistance (Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package	50	10
Junction Temperature Range	-40°C to +125°C	
Operating Temperature Range	-40°C to +85°C	
Storage Temperature Range	-65°C to +150°C	
Pb-free Reflow Profile	see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows:

TA = -40°C to +85°C; VIN = (VO + 0.5V) to 6.5V with a minimum VIN of 2.3V; CIN = 1µF; CO = 1µF; CBYP = 0.01µF; CPOR = 0.01µF.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DC CHARACTERISTICS						
Supply Voltage	VIN		2.3		6.5	V
Ground Current		Quiescent condition: IO1 = 0µA; IO2 = 0µA				
	IDD1	One LDO active		25	32	µA
	IDD2	Both LDO active		42	52	µA
Shutdown Current	IDDS	@ +25°C		0.1	1.0	µA
UVLO Threshold	VUV+		1.9	2.1	2.3	V
	VUV-		1.6	1.8	2.0	V
Regulation Voltage Accuracy		Initial accuracy at VIN = VO + 0.5V, IO = 10mA, TJ = +25°C	-0.7		+0.7	%
		VIN = VO + 0.5V to 5.5V, IO = 10µA to 300mA, TJ = +25°C	-0.8		+0.8	%
		VIN = VO + 0.5V to 5.5V, IO = 10µA to 300mA, TJ = -40°C to +125°C	-1.8		+1.8	%
Maximum Output Current	IMAX	Continuous	300			mA
Internal Current Limit	ILIM		350	475	600	mA
Dropout Voltage (Note 7)	VDO1	IO = 300mA; VO < 2.5V		300	500	mV
	VDO2	IO = 300mA; 2.5V ≤ VO ≤ 2.8V		250	400	mV
	VDO3	IO = 300mA; VO > 2.8V		200	325	mV
Thermal Shutdown Temperature	TSD+			145		°C
	TSD-			110		°C
AC CHARACTERISTICS						
Ripple Rejection (Note 6)		IO = 10mA, VIN = 2.8V(min), VO = 1.8V, CBYP = 0.1µF				
		@ 1kHz		90		dB
		@ 10kHz		70		dB
		@ 100kHz		50		dB
Output Noise Voltage (Note 6)		IO = 100µA, VO = 1.5V, TA = +25°C, CBYP = 0.1µF BW = 10Hz to 100kHz		30		µVRMS

ISL9000A

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows:

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$; $V_{IN} = (V_O + 0.5\text{V})$ to 6.5V with a minimum V_{IN} of 2.3V ; $C_{IN} = 1\mu\text{F}$; $C_O = 1\mu\text{F}$; $C_{BYP} = 0.01\mu\text{F}$; $C_{POR} = 0.01\mu\text{F}$. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DEVICE START-UP CHARACTERISTICS						
Device Enable Time	t_{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the $V_O(\text{nom})$		250	500	μs
LDO Soft-Start Ramp Rate	t_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	60	$\mu\text{s}/\text{V}$
EN1, EN2 PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}		-0.3		0.5	V
Input High Voltage	V_{IH}		1.4		$V_{IN} + 0.3$	V
Input Leakage Current	I_{IL}, I_{IH}				0.1	μA
Pin Capacitance	C_{PIN}	Informative		5		pF
POR1, POR2 PIN CHARACTERISTICS						
$\overline{\text{POR1}}, \overline{\text{POR2}}$ Thresholds	V_{POR+}	As a percentage of nominal output voltage	91	94	97	%
	V_{POR-}		87	90	93	%
$\overline{\text{POR1}}$ Delay	t_{P1LH}		1.0	2.0	3.0	ms
	t_{P1HL}			25		μs
$\overline{\text{POR2}}$ Delay	t_{P2LH}	$C_{POR} = 0.01\mu\text{F}$	100	200	300	ms
	t_{P2HL}			25		μs
$\overline{\text{POR1}}, \overline{\text{POR2}}$ Pin Output Low Voltage	V_{OL}	@ $I_{OL} = 1.0\text{mA}$			0.2	V
$\overline{\text{POR1}}, \overline{\text{POR2}}$ Pin Internal Pull-Up Resistance	R_{POR}		78	100	180	$\text{k}\Omega$

NOTES:

6. Limits established by characterization and are not production tested.
7. $V_{Ox} = 0.98 \cdot V_{Ox}(\text{NOM})$; Valid for V_{Ox} greater than 1.85V.
8. Parts are 100% tested at $+25^{\circ}\text{C}$. Temperature limits established by characterization and are not production tested.

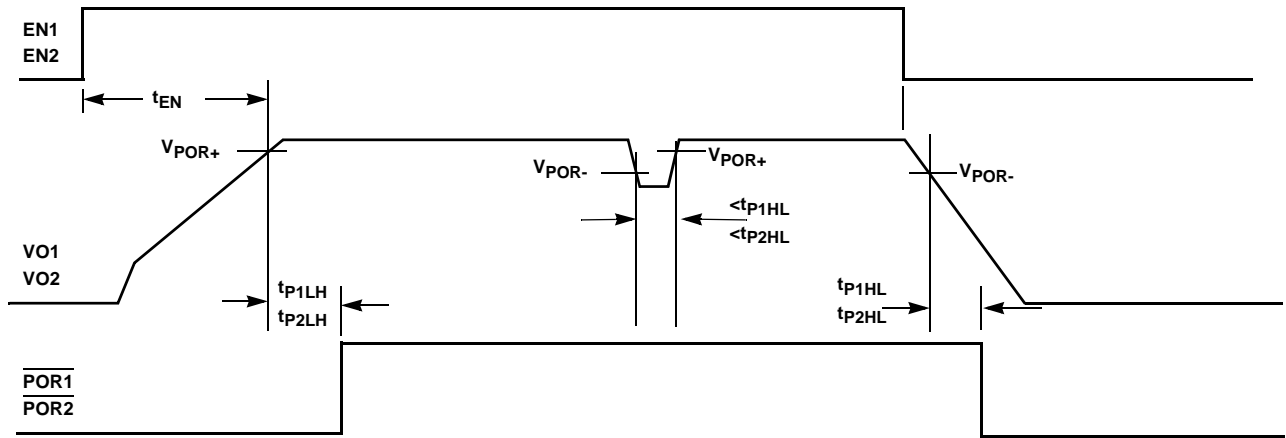


FIGURE 1. TIMING PARAMETER DEFINITION

Typical Performance Curves

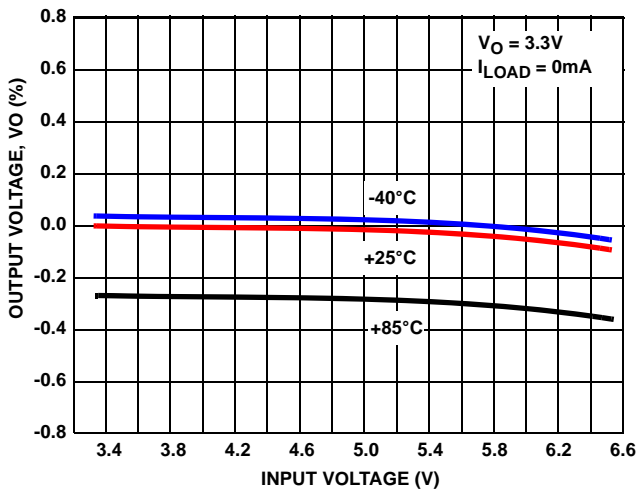


FIGURE 2. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

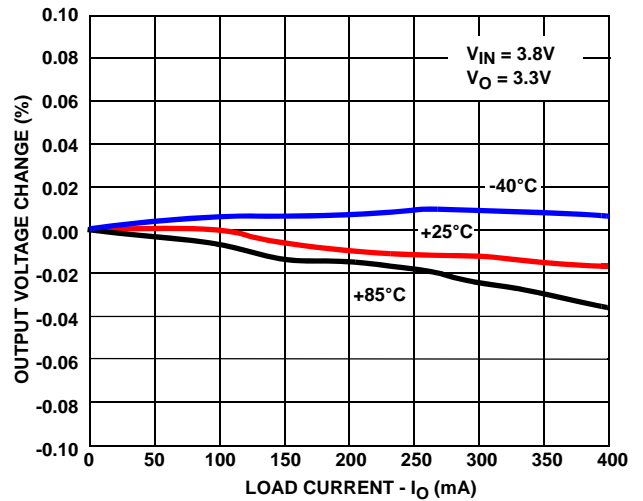


FIGURE 3. OUTPUT VOLTAGE CHANGE vs LOAD CURRENT

Typical Performance Curves (Continued)

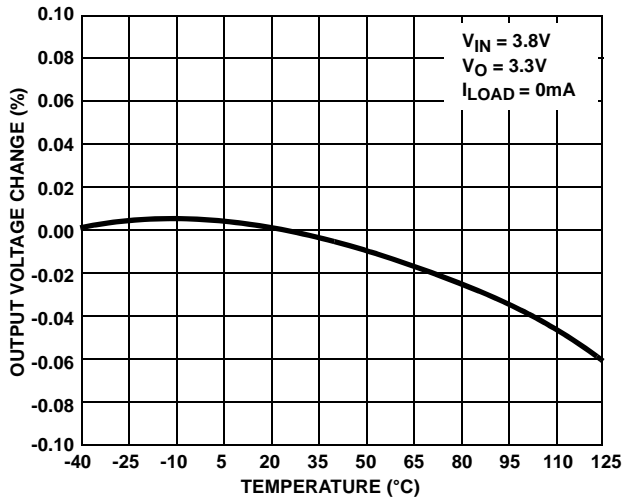


FIGURE 4. OUTPUT VOLTAGE CHANGE vs TEMPERATURE

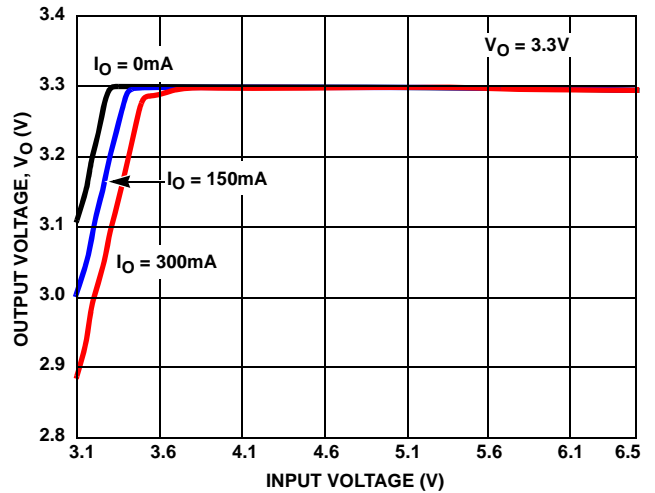


FIGURE 5. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

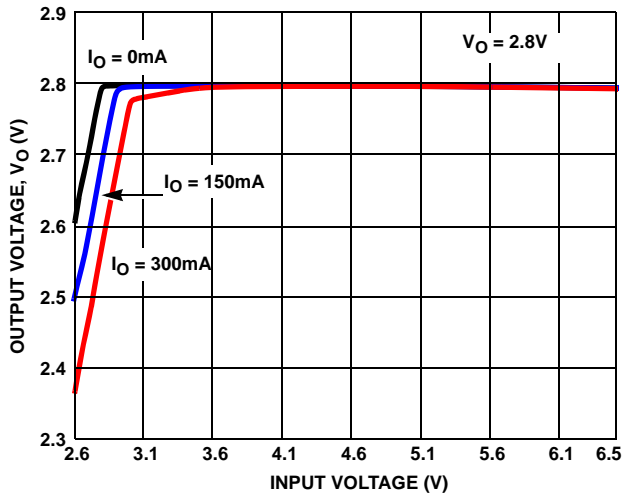


FIGURE 6. OUTPUT VOLTAGE vs INPUT VOLTAGE (2.8V OUTPUT)

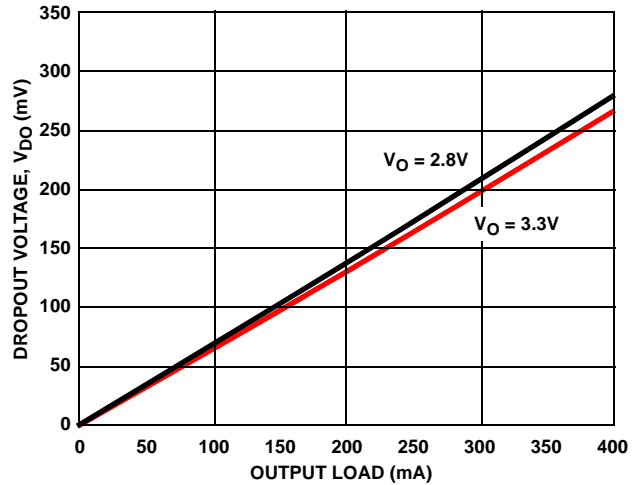


FIGURE 7. DROPOUT VOLTAGE vs LOAD CURRENT

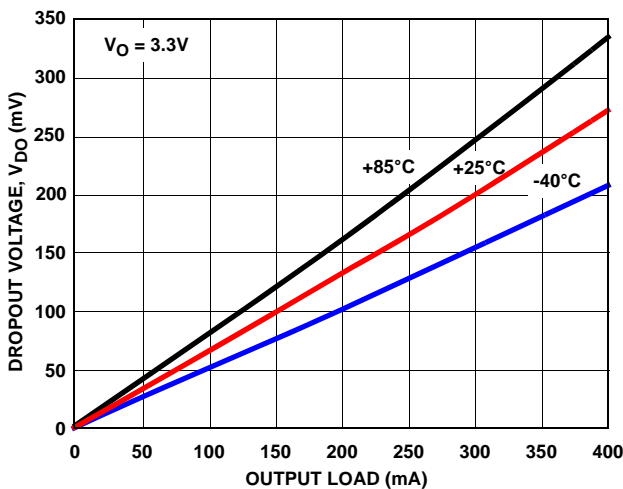


FIGURE 8. DROPOUT VOLTAGE vs LOAD CURRENT

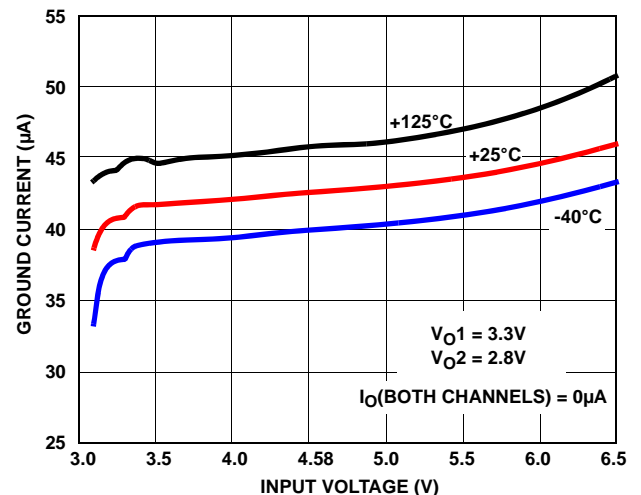


FIGURE 9. GROUND CURRENT vs INPUT VOLTAGE

Typical Performance Curves (Continued)

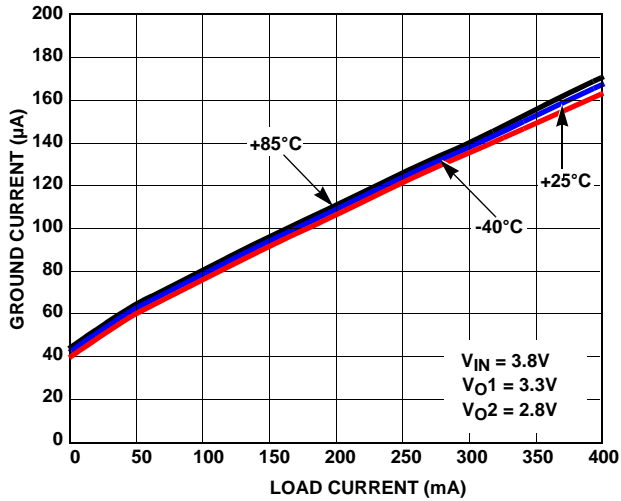


FIGURE 10. GROUND CURRENT vs LOAD

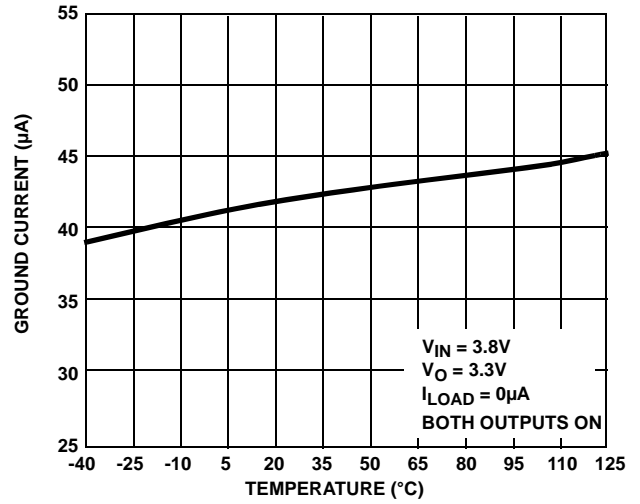


FIGURE 11. GROUND CURRENT vs TEMPERATURE

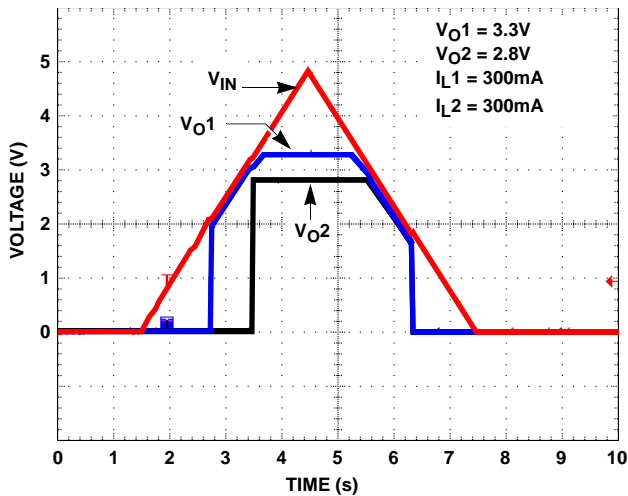


FIGURE 12. POWER-UP/POWER-DOWN

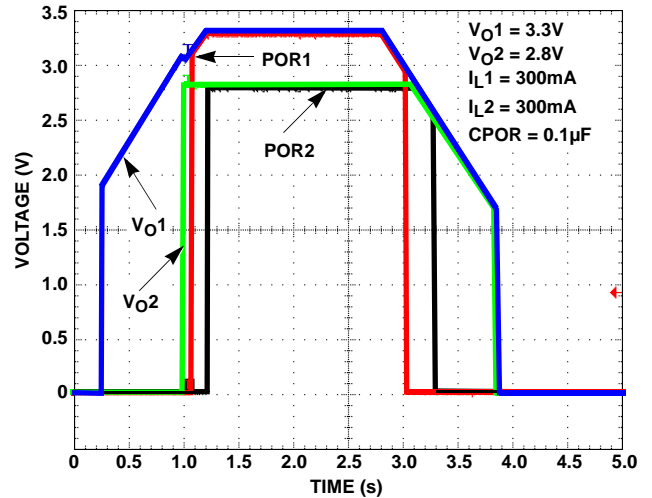


FIGURE 13. POWER-UP/POWER-DOWN WITH POR SIGNALS

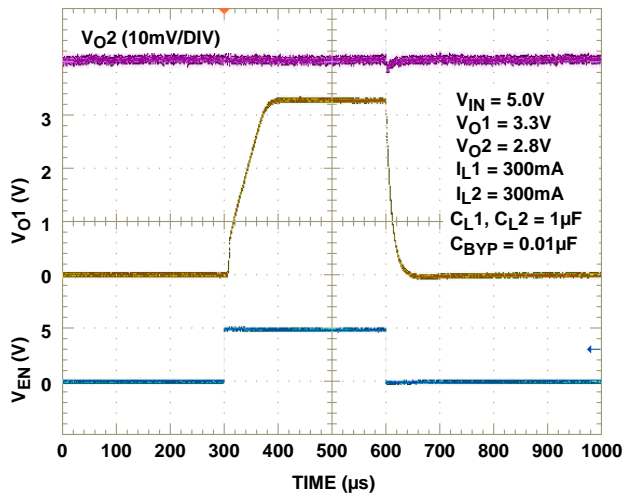


FIGURE 14. TURN-ON/TURN-OFF RESPONSE

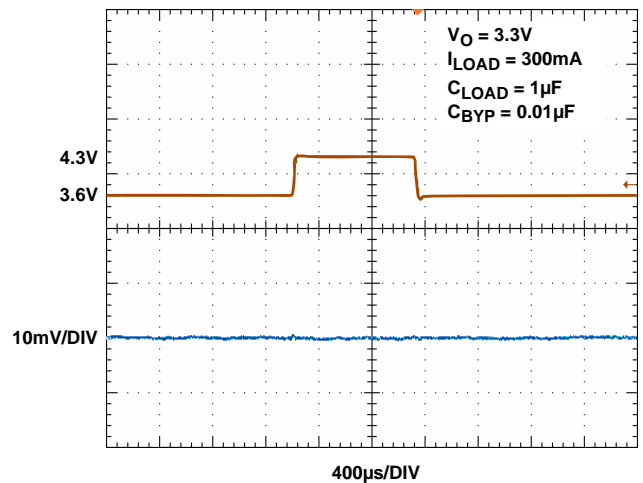


FIGURE 15. LINE TRANSIENT RESPONSE (3.3V OUTPUT)

Typical Performance Curves (Continued)

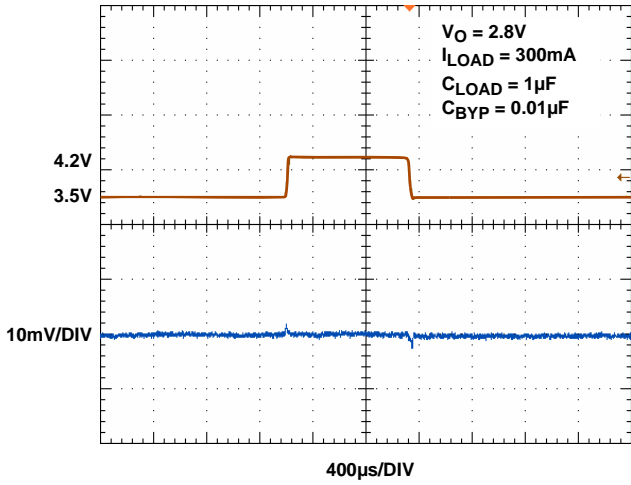


FIGURE 16. LINE TRANSIENT RESPONSE (2.8V OUTPUT)

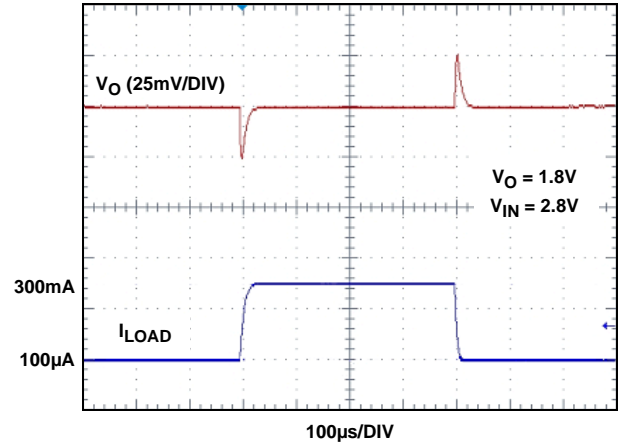


FIGURE 17. LOAD TRANSIENT RESPONSE

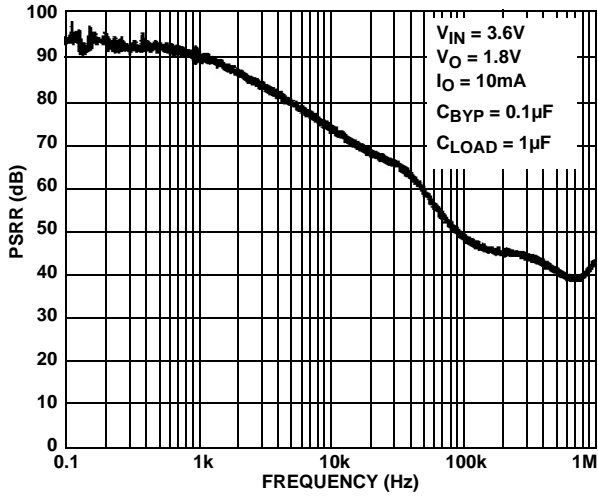


FIGURE 18. PSRR vs FREQUENCY

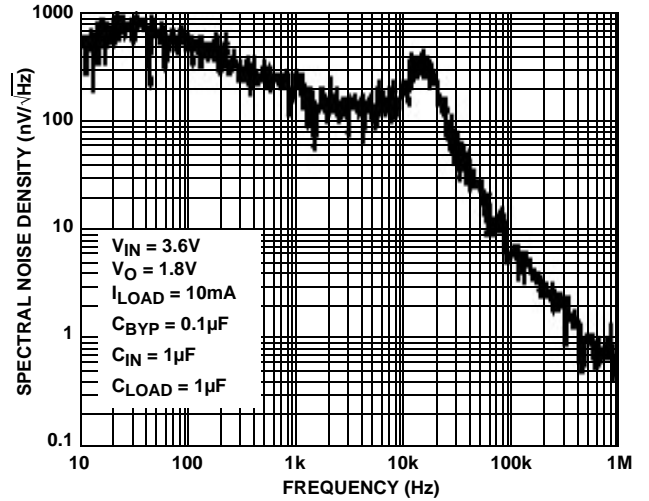
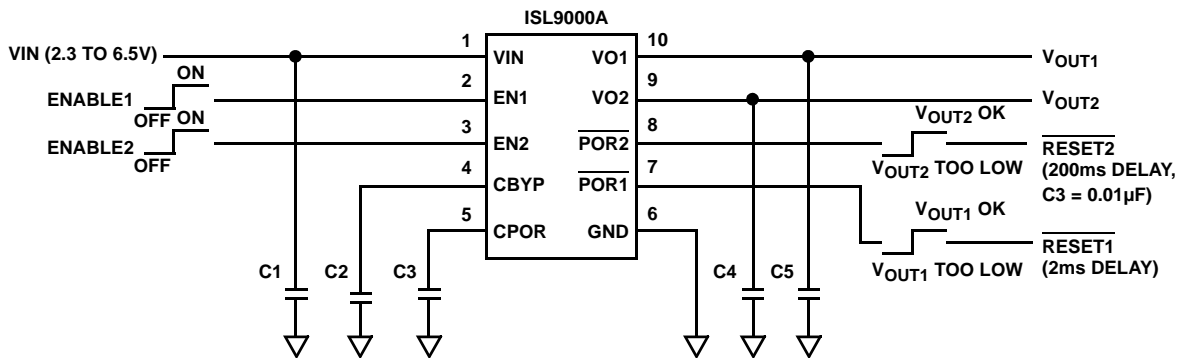


FIGURE 19. SPECTRAL NOISE DENSITY vs FREQUENCY

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VIN	Analog I/O	Supply Voltage/LDO Input: Connect a 1μF capacitor to GND.
2	EN1	Low Voltage Compatible CMOS Input	LDO-1 Enable.
3	EN2	Low Voltage Compatible CMOS Input	LDO-2 Enable.
4	CBYP	Analog I/O	Reference Bypass Capacitor Pin: Optionally connect capacitor of value 0.01μF to 1μF between this pin and GND to tune in the desired noise and PSRR performance.
5	CPOR	Analog I/O	POR2 Delay Setting Capacitor Pin: Connect a capacitor between this pin and GND to delay the $\overline{\text{POR2}}$ output release after LDO-2 output reaches 94% of its specified voltage level. (200ms delay per 0.01μF).
6	GND	Ground	GND is the connection to system ground. Connect to PCB Ground plane.
7	$\overline{\text{POR1}}$	Open Drain Output (1mA)	Open-drain POR Output for LDO-1 (active-low): Internally connected to VO1 through 100kΩ resistor.
8	$\overline{\text{POR2}}$	Open Drain Output (1mA)	Open-drain POR Output for LDO-2 (active-low): Internally connected to VO2 through 100kΩ resistor.
9	VO2	Analog I/O	LDO-2 Output: Connect capacitor of value 1μF to 10μF to GND (1μF recommended).
10	VO1	Analog I/O	LDO-1 Output: Connect capacitor of value 1μF to 10μF to GND (1μF recommended).

Typical Application



C1, C4, C5: 1μF X5R CERAMIC CAPACITOR
 C2: 0.1μF X7R CERAMIC CAPACITOR
 C3: 0.01μF X7R CERAMIC CAPACITOR

If EN1 is brought high, and EN2 goes high before the VO1 output stabilizes, the ISL9000A delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought high, and EN1 goes high before VO2 starts its output ramp, then VO1 turns on first and, the ISL9000A delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought high, and EN1 goes high after VO2 starts its output ramp, then the ISL9000A immediately starts to ramp up the VO1 output.

If both EN1 and EN2 are brought high at the same time, the VO1 output has priority, and is always powered up first.

During operation, whenever the VIN voltage drops below about 1.8V, the ISL9000A immediately disables both LDO outputs. When VIN rises back above 2.1V, the device re-initiates its start-up sequence and LDO operation will resume automatically.

Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter. The filter includes the external capacitor connected to the CBYP pin. A 0.01 μ F capacitor connected CBYP implements a 100Hz lowpass filter, and is recommended for most high performance applications. For the lowest noise application, a 0.1 μ F or greater CBYP capacitor should be used. This filters the reference noise below the 10Hz to 1kHz frequency band, which is crucial in many noise-sensitive applications.

The bandgap generates a zero temperature coefficient (TC) voltage for the reference divider. The reference divider provides the regulation reference, POR detection thresholds, and other voltage references required for current generation and over-temperature detection.

The current generator provides the references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

LDO Regulation and Programmable Output Divider

The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9000A provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1 μ F to 10 μ F output capacitor that has a tolerance better than 20% and ESR less than 200m Ω . The design is performance-optimized for a 1 μ F capacitor. Unless limited by the application, use of an output capacitor value above 4.7 μ F is not normally needed as LDO performance improvement is minimal.

Each LDO uses an independently trimmed 1V reference. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation.

The resistor division ratio is programmed in the factory to one of the following output voltages: 1.5V, 1.8V, 1.85V, 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, and 3.3V.

Power-On Reset Generation

Each LDO has a separate Power-on Reset signal generation circuit which outputs to the respective POR pins. The POR signal is generated as follows:

A POR comparator continuously monitors the output of each LDO. The LDO enters a power-good state when the output voltage is above 94% of the expected output voltage for a period exceeding the LDO PGOOD entry delay time (see the following). In the power-good state, the open-drain POR \bar{x} output is in a high-impedance state. An internal 100k Ω pull-up resistor pulls the pin up to the respective LDO output voltage. An external resistor can be added between the POR \bar{x} output and the LDO output for a faster rise time, however, the POR \bar{x} output should not connect through an external resistor to a supply greater than the associated LDO voltage.

The power-good state is exited when the LDO output falls below 90% of the expected output voltage for a period longer than the PGOOD exit delay time. While power-good is false, the ISL9000A pulls the respective POR pin low.

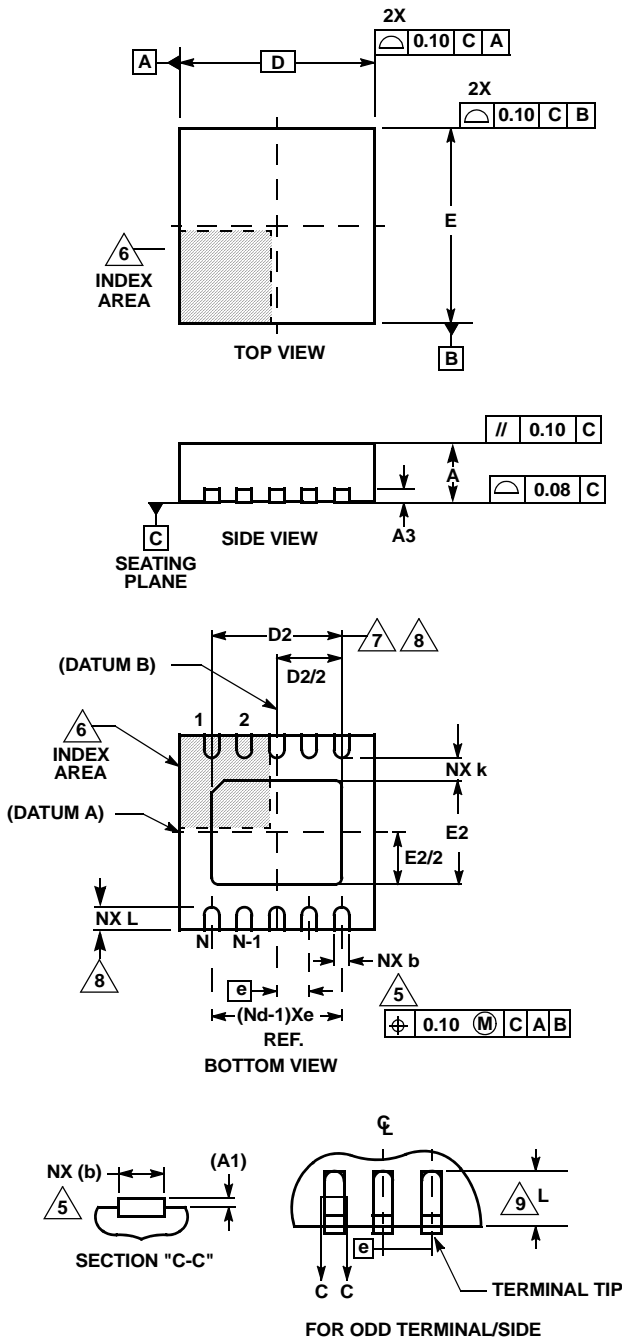
For LDO-1, the PGOOD entry delay time is fixed at about 2ms while the PGOOD exit delay is about 25 μ s. For LDO-2, the PGOOD entry and exit delays are determined by the value of the external capacitor connected to the CPOR pin. For a 0.01 μ F capacitor, the entry and exit delays are 200ms and 25 μ s respectively. Larger or smaller capacitor values will yield proportionately longer or shorter delay times. The POR exit delay should never be allowed to be less than 10 μ s to ensure sufficient immunity against transient induced false POR triggering.

Overheat Detection

The bandgap provides a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about +145 $^{\circ}$ C, one or both of the LDO's momentarily shut down until the die cools sufficiently. In the overheat condition, only the LDO sourcing more than 50mA will be shut off. This does not affect the operation of the other LDO. If both LDOs source more than 50mA and an overheat condition occurs, both LDO outputs are disabled. Once the die temperature falls back below about +110 $^{\circ}$ C, the disabled LDO(s) are re-enabled and soft-start automatically takes place.

The ISL9000A provides short-circuit protection by limiting the output current to about 475mA. If short circuited, an output current of 475mA will cause die heating. If the short circuit lasts long enough, the overheat detection circuit will turn off the output.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3C

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.85	0.90	0.95	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.20	0.25	0.30	5, 8
D	3.00 BSC			-
D2	2.33	2.38	2.43	7, 8
E	3.00 BSC			-
E2	1.59	1.64	1.69	7, 8
e	0.50 BSC			-
k	0.20	-	-	-
L	0.35	0.40	0.45	8
N	10			2
Nd	5			3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.

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